

REMARKS

Claims 1-32 are pending in this application. Claims 1, 5, 15, 19, 24, and 26 are independent claims. Reconsideration and allowance of the present application are respectfully requested.

Claim Rejections

Rejections Under 35 U.S.C. § 103 – Jeong et al. in view of Ivanov et al.

Claims 1-2, 8-16, 22-25, and 28-32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,717,468 (“Jeong et al.”) in view of U.S. Patent No. 6,359,512 (“Ivanov et al.”). This rejection is respectfully traversed.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Applicants respectfully submit that neither Jeong nor Ivanov, alone or in combination, teach or suggest all of the limitations in claim 1. Claim 1 recites: “an operational amplifier; a pull-up transistor connected to an output of the operational amplifier; a pull-down transistor connected to the output of the operational amplifier”. On page 2 of the September 24, 2007 Office Action, the Examiner states that Jeong fails to teach a pull-up and a pull-down transistor connected to an output of the operational transistor. The Examiner further states that Jeong fails to teach a control circuit to selectively actuate the pull-up and pull-down transistors. The Examiner then identifies transistors M11 and M12 in Ivanov (Ivanov: FIGS 1-6) as pull-up and pull-down transistors. However, none of the operational amps in FIGS 1-6 of Ivanov are connected to transistors M11 and M12. With the exception of amplifier 24 in FIGS 1-4, all of the operational amplifiers taught by Ivanov are connected exclusively to the gates of transistors other than M11 or M12 (Ivanov: FIGS 1-6). With respect to amplifier 24, the output of amplifier 24 is connected to the source of transistor M20, not transistor M11 or transistor M12. Even if,

for the sake of argument, amplifier 24 can be said to be connected to pull-down transistor M12 despite being connected to transistor M20, the AB control circuit exists between gate M11 and M12 and Ivanov is silent as to whether or not there is an actual connection between the upper and lower terminals of the AB control circuit. Thus, Ivanov clearly does not teach or suggest any connection between the output of amplifier 24 and the pull-up transistor M11. Accordingly, Ivanov does not teach an operational amplifier the output of which is connected to a pull-up transistor *and* a pull-down transistor as is required by claim 1. Consequently, neither Jeong nor Ivanov, alone or in combination, teach or suggest all of the limitations in claim 1.

Furthermore, the Applicants respectfully submit that the Examiner failed to cite any suggestion or motivation to combine Jeong and Ivanov. On pages 2 and 3 of the September 24, 2007 Office Action, the Examiner simply states: "Thus it would have been obvious to one of ordinary skill in the art to modify the system Jeong et al with the above noted teachings of Ivanov et al such that to provide a push-pull transistor which is selectively controlled by a control circuit connected to an output of the operational amplifier circuit of Jeong et al because both references are related to a high slew rate amplifying circuit". However, the Examiner does not state how one of ordinary skill in the art would combine the teachings of Jeong and Ivanov or even why one of ordinary skill in the art would be motivated to do so. Accordingly, the Examiner failed to cite any suggestion or motivation to combine the references.

For at least the reasons stated above, the Examiner has failed to establish a *prima facie* case of obviousness as is required to support a rejection under §103(a).

Therefore, Applicants respectfully request that this rejection of claims 1-2, 8-16, 22-25, and 28-32 under 35 U.S.C. §103 be withdrawn.

Allowable Subject Matter

Applicants note with appreciation the Examiner's indication that claims 5-7, 19-21, and 26-27 are allowed and that claims 3-4 and 17-18 would be allowable if rewritten in independent form, as they are currently dependent on a rejected base claim.

CONCLUSION

In view of the above remarks and amendments, Applicants respectfully submit that each of the rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Pursuant to 37 C.F.R. §1.17 and 1.136(a), Applicant(s) hereby petition(s) for a one (1) month extension of time for filing a reply to the outstanding Office Action and submit the required \$120.00 extension fee herewith.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,
HARNESS, DICKEY, & PIERCE, P.L.C.

By

John A. Castellano, Reg. No. 35,094

P.O. Box 8910

Reston, Virginia 20195

(703) 668-8000

JHA
JAC/JHA/mat